Appl. No. 10/623,846
Amdt. Dated October 28, 2004
Reply to Office Action of August 2, 2004

## REMARKS

Reconsideration of the application is requested.

Claims 1-2 and 4-9 remain in the application. Claim 1 has been amended. Claim 3 has been canceled.

Under the heading "Claim Rejections - 35 USC § 102" on page 2 of the above-identified Office Action, claims 1-3 have been rejected as being fully anticipated by U.S. Patent No. 5,986,479 to Mohan (hereinafter Mohan) under 35 U.S.C. § 102(b).

The control apparatus recited in claim 1 of the instant application controls the transistor T2 using a control loop. The transistor T2' is a replica transistor, onto which the common source potential Vs of the differential pair is mapped on the replica transistor T2'. This is done via a transistor T11' that is connected in series with T2'. A gate of the transistor T11' is driven such that the drain potentials Vs of T2 and Vs' of T2' are largely the same. The output current on the drain side of the series circuit formed by T2' and T11' in this case largely corresponds to a tail current IT of the differential pair, that is to say it is a replica of it.

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The first current source IQ1 supplies the control loop with a current which corresponds to the sum of the (possibly scaled by a factor) nominal value IS of the foot current, in this case chosen by way of example to be IS/2, and the operating current IB of the control loop. Its operating current IB is drawn once again from the control loop via the second current source IQ2. The gate potential VB2 at the common gate connection of T2 and T2' rises when the replicated current IT/2 is less than the nominal current IS/2, and falls when it is greater than it. This control rule regulates the gate potential VB2 such that the tail current IT corresponds to the nominal current IS. In other words, the control apparatus replicas the current IT traversing the differential pair T11, T12. Claim 1 of the instant application has been amended to recite this feature. Support for this change comes from original claim 3 which has been canceled.

The circuit taught in Mohan is respectfully not believed to teach that the control apparatus M8-M14 replicates the current coming through the COM node of the amplifier M1, M2, M3, M5. Applicants agree with the Examiner's statement that M11 replicates the current  $I_{BG}$  and that M13 replicates a multiple of  $I_{BG}$ . However, this is not what is claimed in claim 1 of the instant application. To be equivalent M11 would have to replicate the current in the amplifier as seen

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at the COM node. Simply put, Mohan is not believed to teach this feature.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 4, and 9. Claims 1, 4, and 9 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on either claim 1 or claim 4.

In view of the foregoing, reconsideration and allowance of claims 1-2 and 4-9 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099. Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to

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the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted

For Applicant

REL:cgm

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